WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a first semiconductor chip including a memory section, input/output sections, a CPU core and a first debug circuit section for verifying operation of a program executed by the CPU core; and

a second semiconductor chip retained over a principal surface of the first semiconductor chip and including a second debug circuit section electrically connected to the CPU core and the first debug circuit section,

wherein the first debug circuit section includes a command analyzing section for analyzing a debug command input from outside, a first transmitting/receiving section for, if the analyzed command is a command to be executed by the CPU core, transmitting the command to the CPU core and receiving an execution result of the command from the CPU core, and a second transmitting/receiving section for, if the analyzed command is a command to be executed by the second debug circuit section, transmitting the command to the second debug circuit section and receiving an execution result of the command from the second debug circuit, and

the second debug circuit section includes a debugging function circuit.

2. The semiconductor integrated circuit device of claim 1, wherein the debugging function circuit includes at least one of a watch point circuit, a trace circuit, a timer circuit, a trigger circuit and a cache information circuit, and is configured by selecting said one circuit from a plurality of circuits having a single function and mutually differing in scale and configuration.

3. The semiconductor integrated circuit device of claim 1, wherein the debugging

function circuit is a rewritable hardware circuit.

4. A semiconductor integrated circuit device, comprising:

a first semiconductor chip including a memory section, input/output sections, a first CPU core, a first debug circuit section for verifying operation of a program executed by the first CPU core, a second CPU core, and a second debug circuit section for verifying operation of a program executed by the second CPU core;

a second semiconductor chip retained over a principal surface of the first semiconductor chip and including a third debug circuit section electrically connected to the first CPU core and the first debug circuit section;

a third semiconductor chip retained over the principal surface of the first semiconductor chip and including a fourth debug circuit section electrically connected to the second CPU core and the second debug circuit section; and

a command switching section for switching a debug command input from outside, between the first debug circuit section and the second debug circuit section,

wherein the first debug circuit section includes a command analyzing section for analyzing the debug command input through the command switching section, a first transmitting/receiving section for, if the analyzed command is a command to be executed by the first CPU core, transmitting the command to the first CPU core and receiving an execution result of the command from the first CPU core, and a second transmitting/receiving section for, if the analyzed command is a command to be executed by the third debug circuit section, transmitting the command to the third debug circuit section and receiving an execution result of the command from the third debug circuit,

the second debug circuit section includes a command analyzing section for analyzing the debug command input through the command switching section, a third

transmitting/receiving section for, if the analyzed command is a command to be executed by the second CPU core, transmitting the command to the second CPU core and receiving an execution result of the command from the second CPU core, and a fourth transmitting/receiving section for, if the analyzed command is a command to be executed by the fourth debug circuit section, transmitting the command to the fourth debug circuit section and receiving an execution result of the command from the fourth debug circuit, and

each of the third and fourth debug circuit sections includes a debugging function circuit.

5. The semiconductor integrated circuit device of claim 4, wherein the debugging function circuit includes at least one of a watch point circuit, a trace circuit, a timer circuit, a trigger circuit and a cache information circuit, and is configured by selecting said one circuit from a plurality of circuits having a single function and mutually differing in scale and configuration.

6. The semiconductor integrated circuit device of claim 4, wherein the debugging function circuit is a rewritable hardware circuit.

7. A debugger device issuing an instruction to first and second debug circuit sections in a semiconductor integrated circuit device which includes a first semiconductor chip including a memory section, input/output sections, a CPU core and the first debug circuit section and a second semiconductor chip retained over a principal surface of the first semiconductor chip and including the second debug circuit section, the first debug circuit section verifying operation of a program executed by the CPU core, the second

debug circuit section being electrically connected to the CPU core and the first debug circuit section,

the debugger device comprising:

an incorporated debugging-function managing section for identifying a debugging function held in the second debug circuit section; and

a debugger body initializing section for initializing the debugger device based on the identified debugging function.

8. The debugger device of claim 7, wherein the second semiconductor chip in the semiconductor integrated circuit device includes a rewritable hardware circuit,

the debugger device includes:

a hardware information managing section for managing information on the hardware circuit;

a debugging function construction judging section for judging at least one debugging function included in the hardware circuit whether or not said at least one debugging function is incorporable; and

a debugging function constructing section for constructing, in the hardware circuit, a debugging function judged to be incorporable by the debugging function construction judging section.

9. The debugger device of claim 8, wherein the debugging function constructing section selects one circuit from among a plurality of hardware circuits created as circuit data beforehand.

10. The debugger device of claim 9, further including a debug-setting-information

managing section for storing the debug information set in the hardware circuit,

wherein the debug-setting-information managing section cancels the debugging information set in the hardware circuit and then resets, in the hardware circuit, the debugging information stored in the debug-setting-information managing section.

11. The debugger device of claim 8, wherein the debugging function constructing section includes a debugging function information managing section for holding a plurality of debugging functions, and

the hardware information managing section holds a plurality of pieces of hardware circuit information.